AN2782
Application note

Solution for designing a 400 W fixed-off-time controlled PFC preregulator with the L6562A

Introduction

In addition to the transition mode (TM) and fixed-frequency continuous conduction mode (FF-CCM) operation of PFC pre-regulators, a third approach is proposed that couples the simplicity and affordability of TM operation with the high-current capability of FF-CCM operation. This solution is a peak current-mode control with fixed off-time (FOT). Design equations are given and a practical design for a 400 W board is illustrated and evaluated. Two methods of controlling power factor corrector (PFC) pre-regulators based on boost topology are currently in use: the fixed-frequency (FF) PWM and the transition mode (TM) PWM (fixed on-time, variable frequency). The first method employs average current-mode control, a relatively complex technique requiring sophisticated controller ICs (e.g. the L4981A/B from STMicroelectronics) and a considerable component count. The second one uses the simpler peak current-mode control, which is implemented with cheaper controller ICs (e.g. the L6561, L6562, L6562A from STMicroelectronics), much fewer external parts and is therefore much less expensive. In the first method the boost inductor works in continuous conduction mode (CCM), while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition. For a given power throughput, TM operation involves higher peak currents as compared to FF-CCM (*Figure 1* and *2*).

Figure 1. Line, inductor, switch and diode currents in FF-CCM PFC

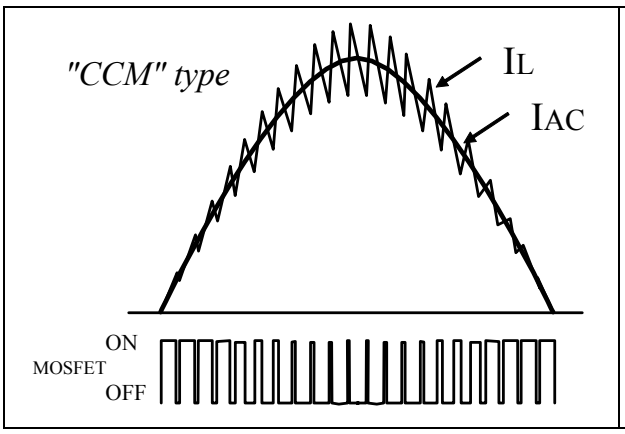
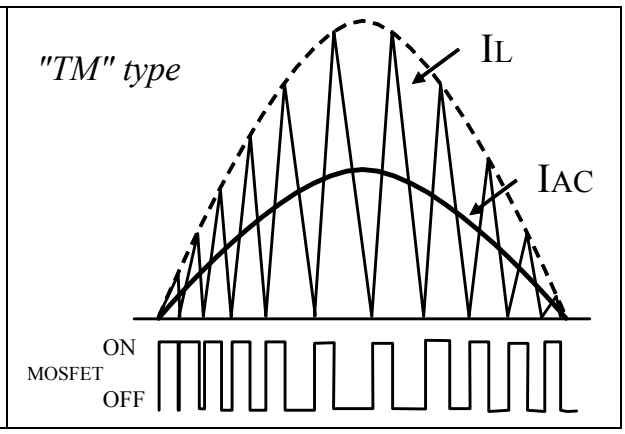


Figure 2. Line, inductor, switch and diode currents in TM PFC



This demonstration, consistent with the above mentioned cost considerations, suggests the use of TM in a lower power range, while FF-CCM is recommended for higher power levels. This criterion, though always true, is sometimes difficult to apply, especially for a midrange power level, around 150-300 W. The assessment of which approach gives the better cost/performance trade-off needs to be done on a case-by-case basis, considering the cost and the stress of not only power semiconductors and magnetic but also of the EMI filter. At the same power level, the switching frequency component to be filtered out in a TM system is twice the line current, whereas it is typically 1/3 or 1/4 in a CCM system.

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1 Introduction to FOT control

In this area where the TM/CCM usability boundary is uncertain, a third approach that couples the simplicity and affordability of TM operation with the high-current capability of CCM operation can be a solution to the dilemma. Generally speaking, FF PWM is not the only alternative when CCM operation is desired. FF PWM modulates both switch ON and OFF times (their sum is constant by definition), and a given converter operates in either CCM or DCM depending on the input voltage and the loading conditions. Exactly the same result can be achieved if the ON-time only is modulated and the OFF-time is kept constant, in which case, however, the switching frequency is no longer fixed (*Figure 3* and *Figure 4*). This is referred to as “fixed off-time” (FOT) control. Peak-current-mode control can still be used.

Figure 3. Basic waveforms for fixed-frequency PWM

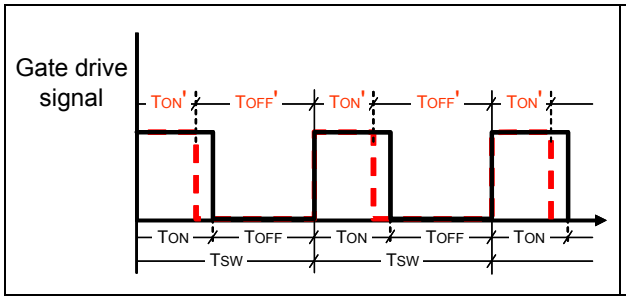
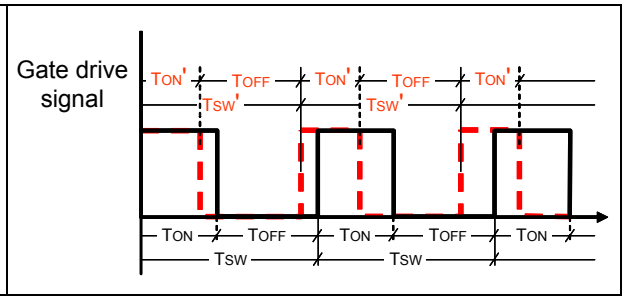


Figure 4. Basic waveforms for fixed off-time PWM

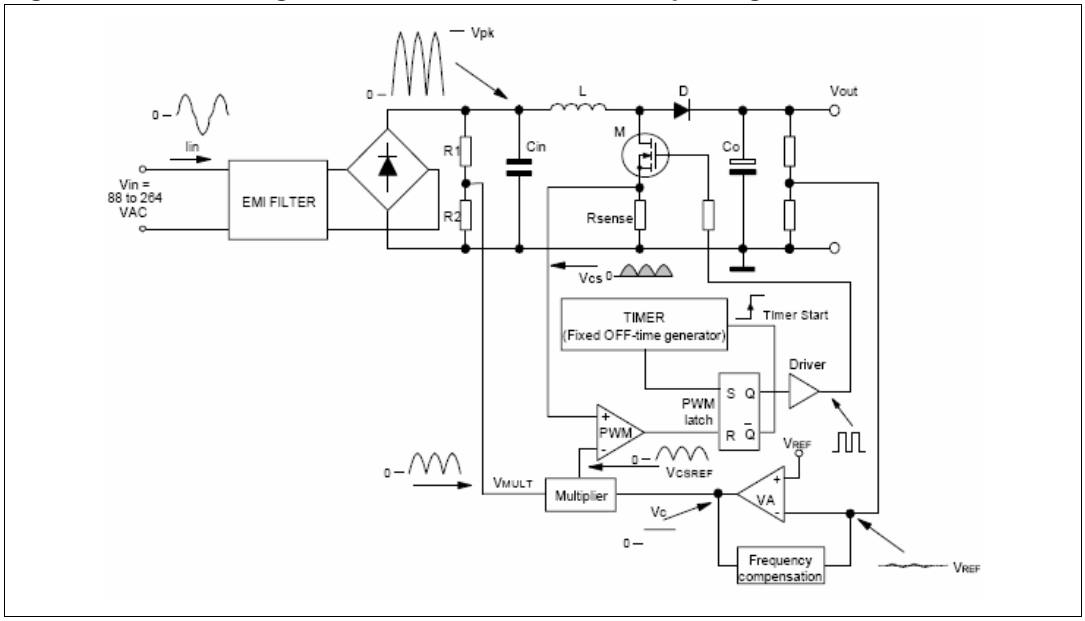


An important point is that FOT control does not need a specialized control IC. A simple modification of a standard TM PFC controller operation, requiring just a few additional passive parts and no significant extra cost, is all that is needed.

2 Operation of an FOT-controlled PFC pre-regulator

Figure 5 shows a block diagram of an FOT-controlled PFC pre-regulator. An error amplifier (VA) compares a portion of the pre-regulator's output voltage Vout with a reference VREF and generates an error signal V_C proportional to their difference. VC, a DC voltage by hypothesis, is fed into an input of the multiplier block and multiplied by a portion of the rectified input voltage V_{MULT}. At the output of the multiplier, there will be a rectified sinusoid, V_{CSREF}, whose amplitude is proportional to that of V_{MULT} and to V_C, which represents the sinusoidal reference for PWM modulation. V_{CSREF} is fed into the inverting input of a comparator that, on the non-inverting input, receives the voltage V_{CS} on the sense resistor Rsense, proportional to the current flowing through the switch M (typically a MOSFET) and the inductor L during the ON-time of M. When the two voltages are equal, the comparator resets the PWM latch and M, supposedly already ON, is switched off.

Figure 5. Block diagram of an FOT-controlled PFC pre-regulator



As a result, V_{CSREF} determines the peak current through M and the inductor L. As V_{CSREF} is a rectified sinusoid, the inductor peak current is enveloped by a rectified sinusoid as well. The line current Iin will be the average inductor current that is the low-frequency component of the inductor current resulting from the low-pass filtering operated by the EMI filter.

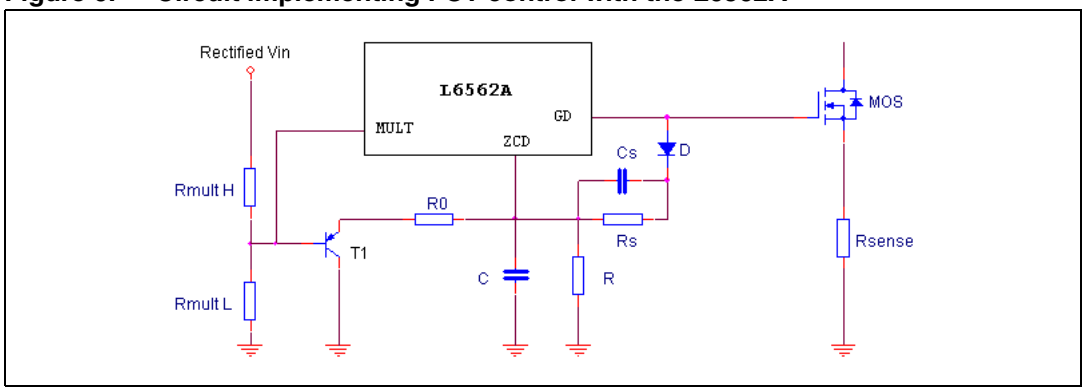
The PWM latch output Q going high activates the timer that, after a predetermined time T_{OFF} has elapsed, sets the PWM latch, thus turning M on and starting another switching cycle. If T_{OFF} is such that the inductor current does not fall to zero, the system operates in CCM. It is apparent that FOT control requires nearly the same architecture as TM control, just the way the off-time of M is determined changes. It is not a difficult task to modify externally the operation of the standard TM PFC controller so that the off-time of M is fixed. As a controller we will refer to the L6562A [4], which is suitable for a few hundred watts power applications because of its gate drive capability and its high noise immunity.

For a more detailed and complex description of the fixed off-time technique and in particular the line modulated FOT, please refer to [7].

3 The circuit implementing the line-modulated fixed off-time with the new L6562A

The circuit that implements LM-FOT control with the L6562A is shown in *Figure 6*. During the ON-time of the MOSFET the gate voltage V_{GD} = 15 V is high, the diode D is forward-biased and the voltage at the ZCD pin is internally clamped at $V_{ZCDclamp} \approx 5.7$ V. During the off-time of M V_{GD} = 10 V is low, the diode D is reverse-biased and the voltage at the pin decays with an exponential law until it reaches the triggering threshold ($V_{ZCDtrigger} \approx 0.7$ V) that causes the switch to turn on. The time needed for the ZCD voltage to go from $V_{ZCDclamp}$ to $V_{ZCDtrigger}$ defines the duration of the off-time T_{OFF}.

Figure 6. Circuit implementing FOT control with the L6562A



The circuit of *Figure 6* makes T_{OFF} a function of the RMS line voltage thanks to the peak-holding effect of T1 (which acts as a buffer) along with R and C whose time constant is significantly longer than a line half-cycle. With the addition of R_0 and T, as long as the voltage on the ZCD pin during T_{OFF} is above $V_{mult}+V_{BE}$, C is discharged through R and R0, following the law:

$$V'_{ZCD}(t) = \left[V_{ZCDclamp} - \frac{R}{R_0 + R} \cdot \left(V_{mult} + V_{BE}\right) \right] \cdot e^{-\frac{t \cdot (R+R_0)}{(RR_0) \cdot C}} + \frac{R}{R_0 + R} \cdot \left(V_{mult} + V_{BE}\right) \quad (1)$$

As $V'_{ZCD}(t)$ falls below $V_{mult}+V_{BE}$, T1 is cut off and C is discharged through R only, so that its evolution from that point on is described by:

$$V''_{ZCD}(t) = \frac{R}{R_0 + R} \cdot \left(V_{mult} + V_{BE}\right) \cdot e^{-\frac{t}{R \cdot C}} \quad (2)$$

$V'_{ZCD}(t)$ decreases from $V_{ZCDclamp}$ = 5.7 V to $V_{mult}+V_{BE}$ in the following time period t':

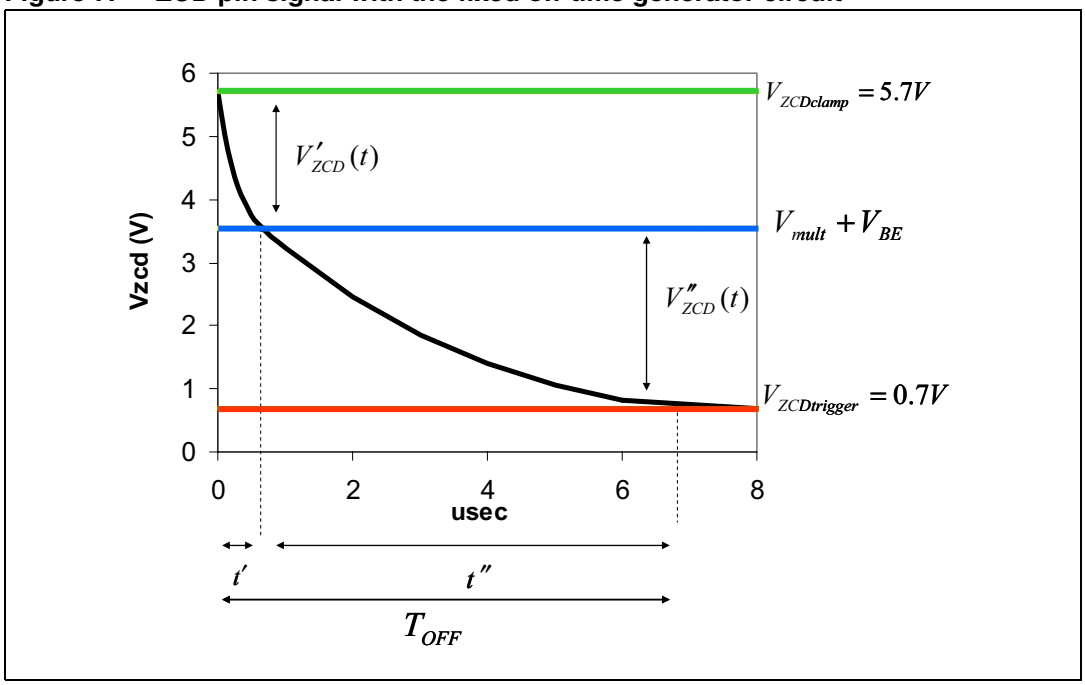
$$t' = -\frac{R \cdot R_0}{R + R_0} \cdot C \cdot \ln\left[\frac{\left(V_{mult} + V_{BE}\right) \cdot R_0}{V_{ZCDclamp} \cdot (R + R_0) - \left(V_{mult} + V_{BE}\right) \cdot R} \right] \quad (3)$$

and $V''_{ZCD}(t)$ decreases from $V_{mult}+V_{BE}$ to $V_{ZCDtriggering}$ = 0.7 V level in the following time period t'':

$$t'' = -RC \cdot \ln\left[\frac{V_{ZCDtrigger}}{V_{mult} + V_{BE}}\right] \quad (4)$$

Figure 7 illustrates the signal on the ZCD pin with the two discharging time constants depending on the two resistors R, R_0 and the L6562A parameters, particularly the upper clamp voltage and the triggering voltage of the ZCD pin.

Figure 7. ZCD pin signal with the fixed off-time generator circuit



The sum of the two time periods is the OFF-time function:

$$T_{OFF} = -RC \cdot \left[\frac{R_0}{R + R_0} \cdot \ln\left[\frac{(V_{mult} + V_{BE}) \cdot R_0}{V_{ZCDclamp} \cdot (R + R_0) - (V_{mult} + V_{BE}) \cdot R}\right] + \ln\left(\frac{V_{ZCDtrigger}}{(V_{mult} + V_{BE})}\right)\right] \quad (5)$$

In this way, once the multiplier operating point (that is, the V_{mult} /VAC ratio) is fixed, with a proper selection of R and R_0 it is possible to increase T_{OFF} with the line voltage so that, at maximum line voltage, it is always $T_{ON}>T_{ONmin}$ = 450 ns for the L6562A [4]. This is a condition needed in order to avoid line distortion [7].

It is easy to see that T_{OFF} is now a function of the instantaneous line voltage. We will refer to this technique as “line-modulated fixed off-time” (LM-FOT) [7].

This modification, though simple, introduces profound changes in the timing relationships, with a positive influence on the energetic relationships. From the control point of view, modulating T_{OFF} is a feedforward term that modifies the gain but does not change its

characteristics. Consequently, all of the properties of the standard FOT control are maintained.

Due to the highly non-linear nature of the T_{OFF} modulation introduced by T1 and R_0, its effects are discussed only qualitatively and the quantitative aspects are provided graphically for a specific case in [7].

As a practical rule, it is convenient to first select a capacitor and then to calculate the resistor needed to achieve the desired T_{OFF} (see *Section 4.3.7*).

As the gate voltage V_{GD} goes high, the resistor Rs charges the timing capacitor C as quickly as possible up to $V_{ZCDclamp}$, without exceeding clamp rating (I_{ZCDx} =10 mA). Then it must fulfill the following inequalities:

$$\frac{V_{GDx} - V_{ZCDclamp} - V_F}{I_{ZCDx} + \frac{V_{ZCDclamp}}{R}} < Rs < R \cdot \frac{V_{GD} - V_{ZCDclamp} - V_F}{V_{ZCDclamp}} \quad (6)$$

where V_{GD} (assume V_{GD} = 10 V) is the voltage delivered by the gate driver, V_{GDx} = 15 V its maximum value, and V_F the forward drop on D.

When working at high line/light load the on-time of the power switch becomes very short and the resistor Rs alone is no longer able to charge C up to $V_{ZCDclamp}$. The speed-up capacitor Cs is then used in parallel to Rs. This capacitor causes an almost instantaneous charge of C up to a level, after that Rs completes the charge up to $V_{ZCDclamp}$. It is important that the steep edge caused by Cs does not reach the clamp level, otherwise the internal clamp of the L6562A undergoes uncontrolled current spikes (limited only by the dynamic resistance of the 1N4148 and the ESR of Cs) that could overstress the IC. Cs must then be:

$$Cs < C \frac{V_{ZCDclamp}}{V_{GDx} - V_{ZCDclamp} - V_F} \quad (7)$$

4 Designing a fixed off-time PFC

4.1 Input specification

The following is a possible design flowchart in reference to a fixed off-time mode PFC using the L6562A. This first part is a detailed specification of the operating conditions of the circuit that is needed for the following calculations in *Section 4.2*. In this example a 400 W, wide input range mains PFC circuit has been considered. Some design criteria are also given.

- Mains voltage range (Vac rms): $VAC_{min} = 90$ Vac $VAC_{max} = 265$ Vac (8)

- Minimum mains frequency: $f_l = 47$ Hz (9)

- Rated output power (W): $P_{out} = 400$ W (10)

Because the PFC is a boost topology the regulated output voltage depends strongly on the maximum AC input voltage. In fact, for correct boost operation the output voltage must always be higher than the input and thus, because Vin max is $VAC_{max} \cdot \sqrt{2} = 374$ V_{pk}, the output has been set at 400 Vdc as the typical value. If the input voltage is higher, as typical in ballast applications, the output voltage must be set higher accordingly. As a rule of thumb the output voltage must be set 6/7% higher than the maximum input voltage peak.

- Regulated DC output voltage (Vdc): $V_{out} = 400$ V (11)

The target efficiency and PF are set here at minimum input voltage and maximum load. They are used for the following operating condition calculation of the PFC. Of course at high input voltage the efficiency is higher.

- Expected efficiency (%): $\eta = \frac{P_{out}}{P_{in}} = 90\%$ (12)

- Expected power factor: $PF = 0.99$ (13)

Because of the narrow loop voltage bandwidth, the PFC output can face overvoltages at startup or in case of load transients. To protect from excessive output voltage that can overstress the output components and the load, the L6562A integrates an OVP. The overvoltage protection sets the extra voltage overimposed to Vout:

- Maximum output overvoltage (Vdc): $\Delta OVP = 40$ V (14)

The mains frequency generates a $2f_L$ voltage ripple on the output voltage at full load. The ripple amplitude determines the current flowing into the output capacitor and the ESR.

Additionally, a certain holdup capability in case of mains dips can be requested from the PFC in which case the output capacitor must also be dimensioned, taking into account the required minimum voltage value (Vout min) after the elapsed holdup time (t_{Hold}).

- Maximum output low frequency ripple: $\Delta V_{out} = 10\ V$ (15)

- Minimum output voltage after line drop (Vdc): $V_{out\,min} = 300V$ (16)

- Holdup capability (ms): $t_{Hold} = 20\ ms$ (17)

The PFC minimum switching frequency is the one of the main parameters used to dimension the boost inductor. Here we consider the switching frequency at low mains on the top of the sinusoid and at full load conditions. As a rule of thumb, it must be higher than the audio bandwidth in order to avoid audible noise and additionally it must not interfere with the L6562A minimum internal starter period, as given in the datasheet. On the other hand, if the minimum frequency is set too high the circuit shows excessive losses at higher input voltage and probably operates skipping switching cycles not only at light load. Typical minimum frequency range is 55÷95 kHz for wide range operation.

- Minimum switching frequency (kHz): $f_{sw\,min} = 72\ kHz$ (18)

Where f_{swmin} = 1/(T+220 nsec) due to the ZCD - gate drive signal delay typical of the L6562A.

The design will be done on the basis of a ripple factor (the ratio of the maximum current ripple amplitude to the inductor peak current at minimum line voltage) k_r=0.36.

- Ripple factor $k_r = 0.34$ (19)

In order to properly select the power components of the PFC and dimension the heat sinks in case they are needed, the maximum operating ambient temperature around the PFC circuitry must be known. Please note that this is not the maximum external operating temperature of the entire equipment, but it is the local temperature at which the PFC components are working.

- Maximum ambient temperature (°C) $T_{ambx} = 50\ °C$ (20)

4.2 Operating condition

The first step is to define the main parameters of the circuit, using the specification points given in *Section 4.1*:

- Rated DC output current

$$I_{out} = \frac{P_{out}}{V_{out}} \quad I_{out} = \frac{400\ W}{400\ V} = 1.00\ A \qquad (21)$$

- Maximum input power

$$P_{in} = \frac{P_{out}}{\eta} \quad P_{in} = \frac{400\ W}{90} \cdot 100 = 444.44\ W \qquad (22)$$

Referring to the main currents shown in *Figure 1*, the following formula expresses the maximum value of current circulating in the boost cell which means at minimum line voltage of the selected range:

- RMS input current

$$I_{in} = \frac{P_{out}}{VAC_{min} \cdot PF} \quad I_{in} = \frac{400\ W}{90Vac \cdot 0.99} = 4.99\ A \qquad (23)$$

It is important to define the following ratios in order to continue describing the energetic relationships in the PFC:

$$k_{min} = \sqrt{2}\frac{VAC_{min}}{V_{out}} \qquad k_{min} = \sqrt{2}\frac{90Vac}{400\ V} = 0.32 \qquad (24)$$

$$k_{max} = \sqrt{2}\frac{VAC_{max}}{V_{out}} \qquad k_{max} = \sqrt{2}\frac{265Vac}{400\ V} = 0.94 \qquad (25)$$

From (24), (25):

- Line peak current:

$$I_{PK\,max} = \frac{2 \cdot P_{in}}{k_{min} \cdot V_{out}} \quad I_{PK\,max} = \frac{2 \cdot (444.44W)}{0.318 \cdot 400V} = 6.98A \qquad (26)$$

- Inductor ripple-ΔILpk:

$$\Delta IL_{pk} = \frac{6 \cdot k_r}{8 - 3 \cdot k_r} \cdot I_{PK\,max} \quad \Delta IL_{pk} = \frac{6 \cdot 0.34}{8 - 3 \cdot 0.34} \cdot 6.98\ A = 2.18\ A \qquad (27)$$

- Inductor peak current: $IL_{pk\,max} = \frac{8}{8 - 3 \cdot k_r} \cdot I_{PK\,max}$ $IL_{pk\,max} = \frac{8}{8 - 3 \cdot 0.34} \cdot 6.98\ A = 8.07\ A$ (28)

It is also possible to calculate the RMS current flowing into the switch and into the diode, needed to calculate the losses of these two elements.

- RMS switch current: $ISW_{rms} = \frac{P_{in}}{k_{min} \cdot V_{out}} \cdot \sqrt{2 - \frac{16 \cdot k_{min}}{3\pi}}$ $ISW_{rms} = \frac{400\ W}{0.318 \cdot 400\ V} \cdot \sqrt{2 - \frac{16 \cdot 0.318}{3\,\pi}} = 4.22\ A$ (29)

- RMS diode current: $ID_{rms} = \frac{P_{in}}{k_{min} \cdot V_{out}} \cdot \sqrt{\frac{16 k_{min}}{3\,\pi}}$ $ID_{rms} = \frac{400\ \ W}{0.318 \cdot 400\ V} \cdot \sqrt{\frac{16 \cdot 0.318}{3\,\pi}} = 2.57\ A$ (30)

It is worth reminding that the accuracy of the approximate energetic relationships described here is quite good at maximum load for low values of the parameter k, that is, at low line voltage, but worsens at high line and as the power throughput is reduced. Since in the design phase current stress is calculated at maximum load and minimum line voltage, their accuracy is acceptable for design purposes.

4.3 Power section design

4.3.1 Bridge rectifier

The input rectifier bridge can use standard slow recovery, low-cost devices.Typically a 600 V device is selected in order to have good margin against mains surges. An NTC resistor limiting the current at turn-on is required to avoid overstress to the diode bridge.

The rectifier bridge power dissipation can be calculated using equations *(31)*, *(32)*, *(33)*. The threshold voltage and dynamic resistance of a single diode of the bridge can be found in the component datasheet.

$$\bar{I}_{inrms} = \frac{\sqrt{2} \cdot I_{in}}{2} = \frac{\sqrt{2} \cdot 4.99\ A}{2} = 3.53\ A \quad (31)$$

$$\bar{I}_{in_avg} = \frac{\sqrt{2} \cdot I_{in}}{\pi} = \frac{\sqrt{2} \cdot 4.99\ A}{\pi} = 2.25\ A \quad (32)$$

The power dissipated on the bridge is:

$$P_{bridge} = 4 \cdot R_{diode} \cdot \bar{I}^2_{inrms} + 4 \cdot V_{th} \cdot \bar{I}_{in_avg}$$
$$P_{bridge} = 4 \cdot 0.025\ \Omega \cdot (3.53A)^2 + 4 \cdot 0.7\ V \cdot 2.25A = 7.53\ W \quad (33)$$

4.3.2 Input capacitor

The input filter capacitor, Cin, is placed across the diode bridge output. This capacitor must smooth the high-frequency ripple and must sustain the maximum instantaneous input voltage. In a typical application an EMI filter is placed between the mains and the PFC circuit. In this application the EMI filter is reinforced by a differential mode Pi-filter after the bridge to reject the differential noise coming from the whole switching circuit.

The design of the EMI filter (common mode and differential mode) is not described here. The value of the input filter capacitor can be calculated as follows, simply considering the output power that the PFC should deliver at full load:

$$C_{in} = 2.5 \cdot 10^{-3} \cdot P_{out} \qquad C_{in} = 2.5 \cdot 10^{-3} \cdot 400\ W = 1\ \mu F \quad (34)$$

The maximum value of this capacitor is limited to avoid line current distortion. The value chosen for this demonstration board is 1 µF.

4.3.3 Output capacitor

The output bulk capacitor (Co) selection depends on the DC output voltage *(11)*, the allowed overvoltage *(14)*, and the converter output power *(10)*.

The 100/120 Hz (twice the mains frequency) voltage ripple (ΔVout = (Vout = peak-to-peak ripple value) *(15)* is a function of the capacitor impedance and the peak capacitor current:

$$\Delta V_{out} = 2 \cdot I_{out} \cdot \sqrt{\frac{1}{(2\pi \cdot 2f_l \cdot C_O)^2} + ESR^2} \quad (35)$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

$$C_O \geq \frac{I_{out}}{2\pi \cdot f_l \cdot \Delta V_{out}} = \frac{P_{out}}{2\pi \cdot f_l \cdot V_{out} \cdot \Delta V_{out}} \qquad C_O \geq \frac{400W}{2\pi \cdot 47Hz \cdot 400V \cdot 10V} = 338\mu F \quad (36)$$

ΔVout is usually selected in the range of 1.5% of the output voltage.

Although ESR usually does not affect the output ripple, it should be taken into account for power loss calculations. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

$$I_{Crms} = \sqrt{ID^2_{rms} - I^2_{out}} \qquad I_{Crms} = \sqrt{(2.56\ A)^2 - (1.0A)^2} = 2.36\ A \quad (37)$$

If the PFC stage has to guarantee a specified holdup time, the selection criterion of the capacitance changes. Co has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage (Vout min) that is the minimum output voltage value (which takes load regulation and output ripple into account). Vout min is the minimum output operating voltage before the 'power fail' detection and consequent stopping by the downstream system supplied by the PFC.

$$C_O = \frac{2 \cdot P_{out} \cdot t_{Hold}}{\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2} \quad C_O = \frac{2 \cdot 400W \cdot 20ms}{(400V - 10V)^2 - (300V)^2} = 242.3\mu F \tag{38}$$

A 20% tolerance on the electrolytic capacitors has to be taken into account for the right dimensioning.

Following the relationship *(38)*, for this application a capacitor Co = 330 µF (450 V) has been selected in order to maintain a holdup capability for 20 ms. The actual output voltage ripple with this capacitor is also calculated. In detail:

$$t_{Hold} = \frac{C_O \cdot \left[\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2\right]}{2 \cdot P_{out}} \tag{39}$$

$$t_{Hold} = \frac{330\ \mu F \cdot \left[(400\ V - 10\ V)^2 - (300\ V)^2\right]}{2 \cdot 400\ W} = 22\ ms$$

As expected, the ripple variation on the output is:

$$\Delta V_{out} = \frac{I_{out}}{2 \cdot \pi \cdot f_l \cdot C_O} \qquad \Delta V_{out} = \frac{1.0\ A}{2 \cdot \pi \cdot 47\ Hz \cdot 330\ \mu F} = 10.2\ V \tag{40}$$

4.3.4 Boost inductor

In the continuous mode approach, the acceptable current ripple factor, Kr, can be considered between 10% to 35%. For this design, the maximum specified current ripple factor is 35%.

To calculate the required inductance L of the boost inductor, use the following formula with a 4.2 µs OFF-time set at 90Vac (see the following ZCD pin dimensioning for finding the correct value):

$$L(VAC) = (1 - k_{min}) \cdot \frac{V_{out}}{\Delta IL_{pk}} T_{OFF}(VAC) \quad L(VAC_{min}) = (1 - 0.32) \cdot \frac{400\ V}{2.11\ A} 4.2\ \mu s = 520\ \mu H \tag{41}$$

After calculating the values of the inductor at low mains and at high mains $L(VAC_{max})$, $L(VAC_{min})$ *(41)* depending also on the OFF-time, the minimum value has to be taken into account. It became the maximum inductance value for the PFC dimensioning.

Figure 8 shows the switching frequency versus the θ angle calculated inverting the *(41)*, with a 500 µH boost inductance and fixing the line voltage at minimum and maximum values.

Figure 8. Switching frequency fixing the line voltage

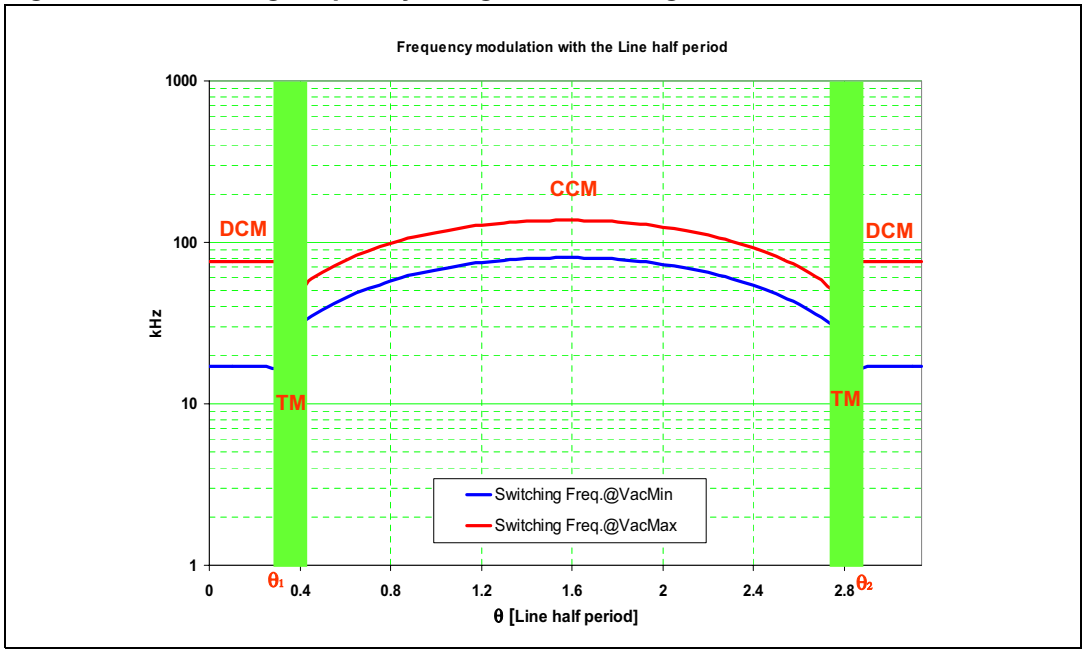
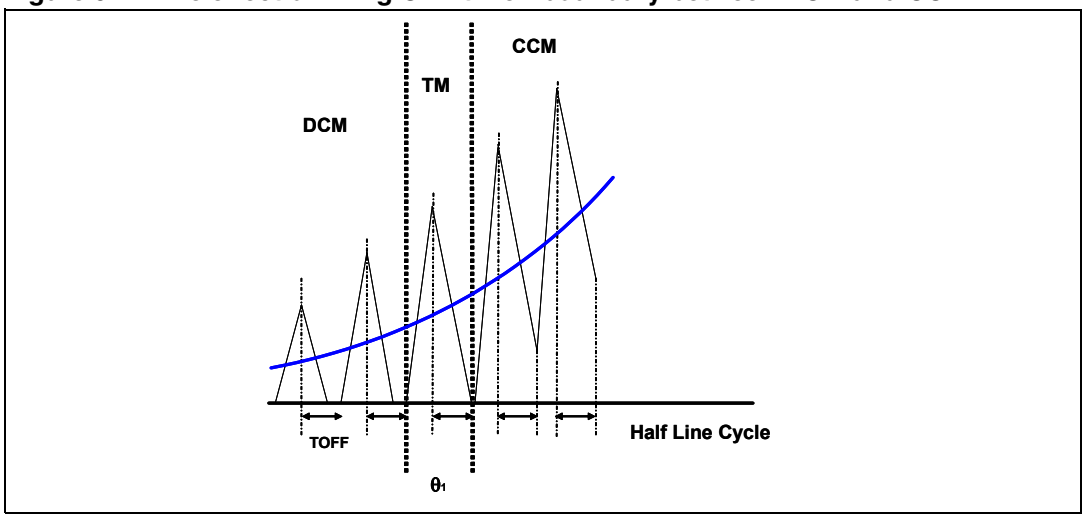


Figure 9. The effect of fixing OFF-time - boundary between DCM and CCM



The effect of fixing the OFF-time is generating a continuous conduction mode in the center region of the line half-cycle between the two transition angles. Close to the zero-crossing, the system works in discontinuous conduction mode and in transition mode at the boundary.

The core size is determined assuming a peak flux density Bx ≅ 0.25 T (depending on the ferrite grade selected and relevant specific losses) and calculating the maximum current according to *(28)* as a function of the maximum current sense pin clamping voltage and sense resistor value.

DC and AC copper losses and ferrite losses must also be calculated to determine the maximum temperature rise of the inductor.

4.3.5 Power MOSFET selection and the dissipation

The selection of the MOSFET concerns mainly its $R_{DS(on)}$, which depends on the output power *(10)*, since the breakdown voltage is fixed just by the output voltage *(11)*, plus the overvoltage allowed *(15)* and a safety margin (20%).

Thus, a voltage rating of 500 V (1.2 · Vout = 480 V) is selected. Using its current rating as a rule of thumb, we can select a device having ~ 3 times the RMS switch current *(29)* but, the power dissipation calculation gives the final confirmation that the selected device is the right one for the circuit also taking into account the heat sink dimensions. In this 400 W TM PFC application two parallel STP12NM50 MOSFETs have been selected in order to support the high inductor current.

The MOSFET's power dissipation depends on conduction, switching and capacitive losses.

The conduction losses at maximum load and minimum input voltage are calculated by:

$$P_{cond}(VAC) = R_{DS(on)} \cdot (ISW_{rms}(VAC))^2 \quad (42)$$

Because normally in the datasheets the $R_{DS(on)}$ is given at ambient temperature (25 °C) to calculate correctly the conduction losses at 100°C (typical MOSFET junction operating temperature), a factor of 1.75 to 2 should be taken into account. The exact factor can be found in the device datasheet.

Now, the conduction losses referred to as 1 Ω $R_{DS(on)}$ at ambient temperature as a function of P_{in} and VAC can be calculated, combining equations *(42)* and *(29)*:

$$P'_{cond}(VAC) = 2 \cdot (ISW_{rms}(VAC))^2 = 2 \cdot \left(\frac{P_{in}}{k(VAC) \cdot V_{out}} \cdot \sqrt{2 - \frac{16 \cdot k(VAC)}{3\,\pi}} \right)^2 \quad (43)$$

The switching losses due to the MOSFET current-voltage I_{MOS}, V_{MOS} crossing occurs at turn-on and turnoff because of the FOT operation and can be basically expressed by:

$$P_{switch}(VAC) = V_{MOS} \cdot I_{MOS} \cdot \left(\frac{t_{rise} + t_{fall}}{2} \right) \cdot f_{sw}(VAC) \quad (44)$$

Because the switching frequency depends on the input line voltage and on the position on the sinusoidal waveform, it can be demonstrated that from *(44)* the switching losses per 1 µs of current rise and fall time can be written as:

$$P'_{switch}(VAC) = V_{out} \cdot \left(IL_{pk\,max} - \frac{\Delta IL_{pk}}{2} \right) \cdot \frac{1}{\pi} \int_0^{\pi} (\sin \vartheta)^2 \cdot f_{sw}(VAC, \theta) \cdot d\vartheta \quad (45)$$

From the selected MOSFET datasheet $t_{rise} = t_{fall}$ = 0.01 µs is the crossover time at turn-on and off.

At turn-on the losses are due to the discharge of the total drain capacitance inside the MOSFET itself.

In general, the capacitive losses are given by:

$$P_{cap}(VAC) = \frac{1}{2} \cdot C_d \cdot V^2_{MOS} \cdot f_{sw}(VAC) \quad (46)$$

where C_d is the total drain capacitance including the MOSFET and the other parasitic capacitances such as inductor etc. At the drain node, V_{MOS} is the drain voltage at MOSFET turn-on.

Taking into account the frequency variation with the input line voltage and the phase angle similar to *(45)*, a detailed description of the capacitive losses per 1 nF of total drain capacitance can be calculated as:

$$P'_{cap}(VAC) = \frac{1}{2} \cdot \frac{1}{\pi} \int_0^{\pi} (V_{out})^2 f_{sw}(VAC, \vartheta) \, d\vartheta \quad (47)$$

The total drain capacitance of the two MOSFETs is //Cd = 0.36 nF, V_{out} is the drain voltage at MOSFET turn-on.

The function of the total losses of the input mains voltage is the sum of the three previous losses from equations *(43)*, *(45)* and *(47)* multiplied for the two parallel MOSFET parameters:

$$P_{loss}(VAC) = RDS_{on} \cdot P'_{cond}(VAC) + \left(\frac{t_{rise} + t_{fall}}{2} \right) \cdot P'_{sw}(VAC) + C_d \cdot P'_{cap}(VAC) \quad (48)$$

From *(48)* using the data relevant to the MOSFET selected and calculating the losses at VACmin and VACmax, we observe that the maximum total losses occurs at VACmin which is 9 W. From this number and the maximum ambient temperature *(20)*, the total maximum thermal resistance required to keep the junction temperature below 125 °C is:

$$R_{th} = \frac{125°C - T_{ambx}}{P_{loss}(VAC)} \qquad R_{th} = \frac{125\ °C - 50\ °C}{9\ W} = 8.1 \frac{°C}{W} \quad (49)$$

If the result of equation *(49)* is lower than the junction-ambient thermal resistance given in the MOSFET datasheet for the selected device package, a heat sink must be used.

Figure 10. Conduction losses and total losses in the two STP12NM50 MOSFETs for the 400 W FOT PFC

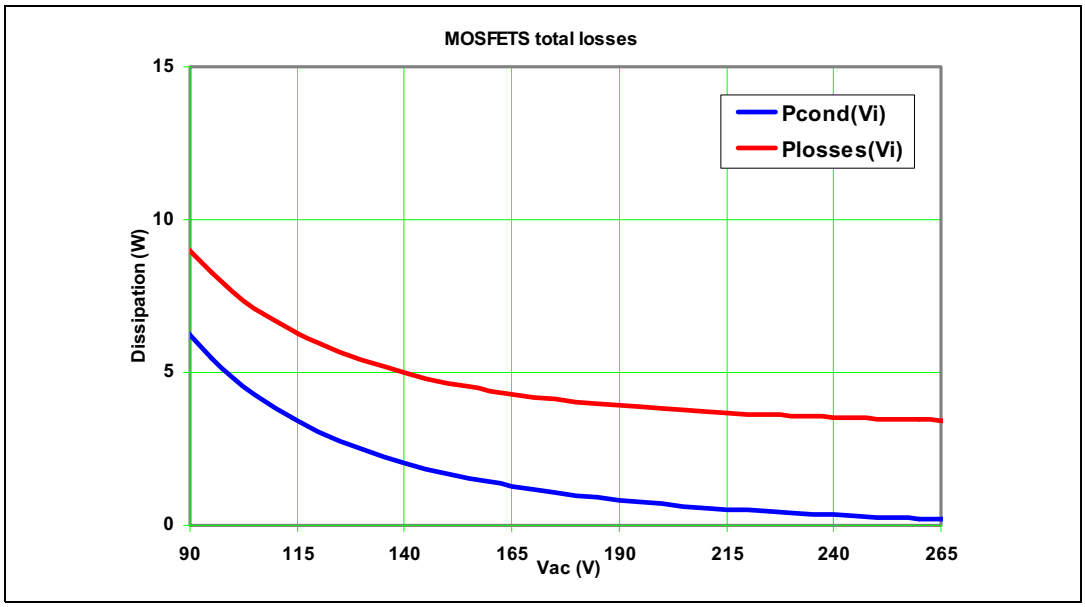


Figure 10 shows the trend of the total losses *(48)* on the line voltage for the two selected STP12NM50 MOSFETs.

4.3.6 Boost diode selection

Following a similar criterion as that for the MOSFET, the output rectifier can also be selected. A minimum breakdown voltage of 1.2·(Vout + ΔOVP) and a current rating higher than 3·Iout *(21)* can be chosen for a rough initial selection of the rectifier. The correct choice is then confirmed by the thermal calculation. If the diode junction temperature works within 125 °C the device has been selected correctly, otherwise a bigger device must be selected.

The switching losses can be significantly reduced if an ultra-fast diode is employed. Since this circuit operates in the continuous current mode, the MOSFET has to recover the boost diode minority carrier charge at turn-on. Thus, a diode with a small reverse recovery time, trr, must be used.

In this 400 W application an STTH8R06, (600 V, 8 A) has been selected. The STTH8R06 offers the best solution for the continuous current mode operation due to its very fast reverse recovery time, 25 ns typical. This part has a breakdown voltage rating (Vrrm) of 600 V, average forward current rating (Ifave) of 8 A and reverse recovery time (trr) of 25 ns.

The rectifier AVG *(21)* and RMS *(30)* current values and the parameter V_{th} (rectifier threshold voltage) and R_d (dynamic resistance) given in the datasheet allow calculating the rectifier losses.

From the STTH8R06 datasheet, V_{th} is 1.16 V, R_d is 0.08 Ω, neglecting the recovery losses:

$$P_{diode} = V_{th} \cdot I_{out} + R_d \cdot ID^2_{rms} \quad P_{diode} = 1.16\ V \cdot 1.0\ A + 0.08\ \Omega \cdot (2.56\ A)^2 = 1.69\ W \qquad (50)$$

From *(20)* and *(50)* the maximum thermal resistance to keep the junction temperature below 125 °C is then:

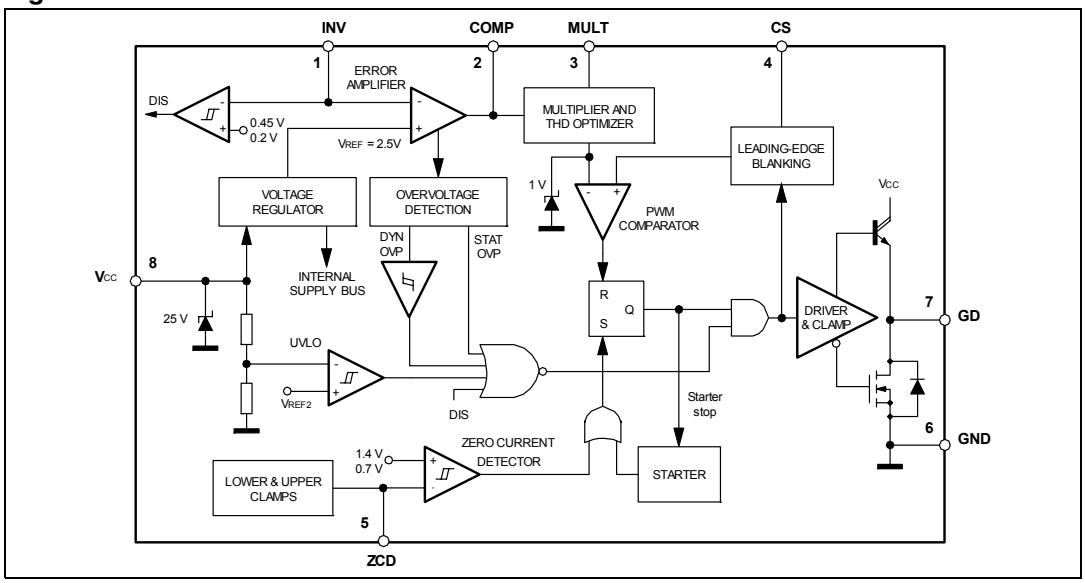
$$R_{th} = \frac{125\ °C - T_{ambx}}{P_{diode}} \qquad R_{th} = \frac{125\ °C - 50\ °C}{1.68\ W} = 44.45\frac{°C}{W} \tag{51}$$

The diode is attached to the same heat sink as the power MOSFET. The STTH8R06 has an isolated package and can be attached directly to the heat sink. Silicone thermal grease may be applied to improve the thermal contact between the diode and heat sink.

4.3.7 L6562A biasing circuitry

Following the dimensioning of the power components, the biasing circuitry for the L6562A is also described. For reference, the internal schematic of the L6562A is represented below in *Figure 11*. For more details on the internal functions, please refer to the datasheet.

Figure 11. L6562A internal schematic



- Pin 1 (INV): This pin is connected both to the inverting input of the E/A and to the OVP circuitry. A resistive divider is connected between the boost regulated output voltage and this pin. The internal reference on the non-inverting input of the E/A is 2.5 V (typ), while the OVP intervention threshold is 27 µA (typ). R_{outH} and R_{outL} are then selected as follows:

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5\ V} - 1 \qquad \frac{R_{outH}}{R_{outL}} = \frac{400\ V}{2.5\ V} - 1 = 159 \tag{52}$$

$$R_{outH} = \frac{\Delta V_{OVP}}{27\ \mu A} \qquad R_{outH} = \frac{40\ V}{27\ \mu A} = 1.481\ M\Omega \tag{53}$$

$$R_{outL} = \frac{R_{outH}}{159} \quad R_{outL} = \frac{R_{outH}}{159} = 9.32\ k\Omega \tag{54}$$

The commercial values selected are R_{outH} = 1530 MΩ and R_{outL} = 9.5 kΩ.

Please note that for R_{outH} a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series have to be used.

This pin can also be used as an ON/OFF control input if tied to GND by an open collector or open drain.

- Pin 2 (COMP): This pin is the output of the E/A that is fed in one of the two inputs of the multiplier. A feedback compensation network is placed between this pin and INV [1]. It has to be designed in with a narrow bandwidth in order to avoid that the system rejects the output voltage ripple (100 Hz) that would bring high distortion of the input current waveform. A theoretical criterion to define the compensation network value is to set the E/A bandwidth (BW) from 20 to 30 Hz.

For a more complex way of compensating the FOT PFC please refer to [1], [2], [3].

A compensated two-pole feedback network for this 400 W FOT PFC has been obtained with the following values:

$$C_{compP} = 220\ nF \quad C_{compS} = 2.2\ \mu F \quad R_{compS} = 47\ k\Omega \tag{55}$$

to which correspond the following open-loop transfer function and its phase function.

Figure 12. Bode plot - open-loop transfer function

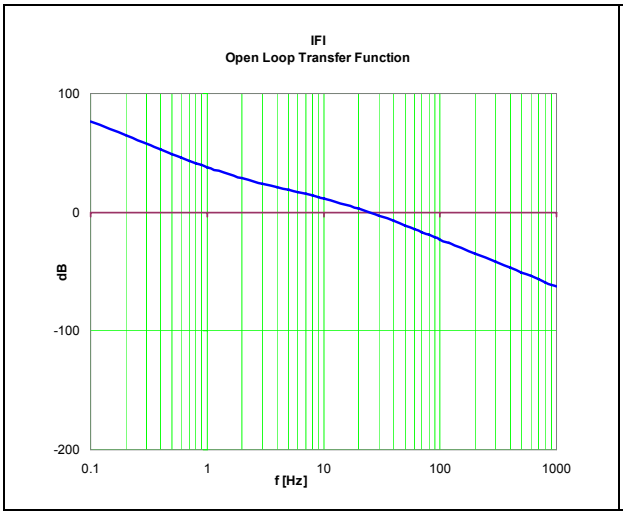
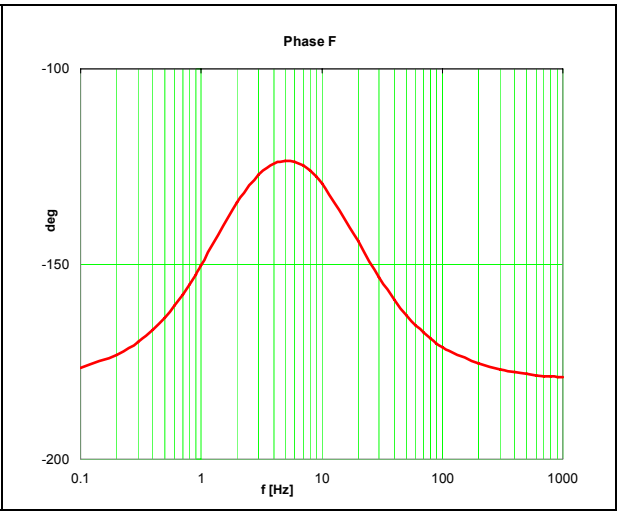


Figure 13. Bode plot - phase



The two bode plot charts are in reference to the PFC operating at the main voltage set point of 265 Vac and full load. In this condition the crossover frequency is fc = 25 Hz, the phase margin is 30 ° and the third harmonic distortion is under 3%.

- Pin 4 (CS): Pin #4 is the inverting input of the current sense comparator. Through this pin, the L6562A reads the instantaneous inductor current, converted to a proportional

voltage by an external sense resistor (R_s). As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET stays in OFF-state until the PWM latch is reset by the ZCD signal. The pin is equipped with 200 ns leading-edge blanking for improved noise immunity.

The sense resistor value (R_s) can be calculated as follows. For the 400 W PFC it is:

$$R_{sx} < \frac{Vcs_{min}}{IL_{pkmax}} \quad R_{sx} < \frac{1.0\ V}{8.07\ A} = 0.124\ \Omega \tag{56}$$

where:

- IL_{pkmax} is the maximum peak current in the inductor, calculated as described in *(28)*
- Vcs_{min} = 1.0 V is the minimum voltage allowed on the L6562A current sense (in the datasheet)

Because the internal current sense clamping sets the maximum current that can flow in the inductor, the maximum peak of the inductor current is calculated considering the maximum voltage Vcs_{max} allowed on the L6562A (in the datasheet):

$$IL_{pksat} = \frac{Vcs_{max}}{R_s} \quad IL_{pksat} = \frac{1.16\ V}{0.12\ \Omega} = 9.67\ A \tag{57}$$

The calculated IL_{pksat} is the limit at which the boost inductor saturates and it is used for calculating the inductor number of turns and air gap length.

The power dissipated in R_s is given by:

$$P_s = R_s \cdot ISW_{rms}^2 \quad P_s = 0.12\ \Omega \cdot (10.54\ A)^2 = 2.14\ W \tag{58}$$

It does not exceed 1% of the rated output power *(10)*, that is, 4 W.

According to the result, four parallel resistors of 0.47 Ω with 1 W of power rating have been selected.

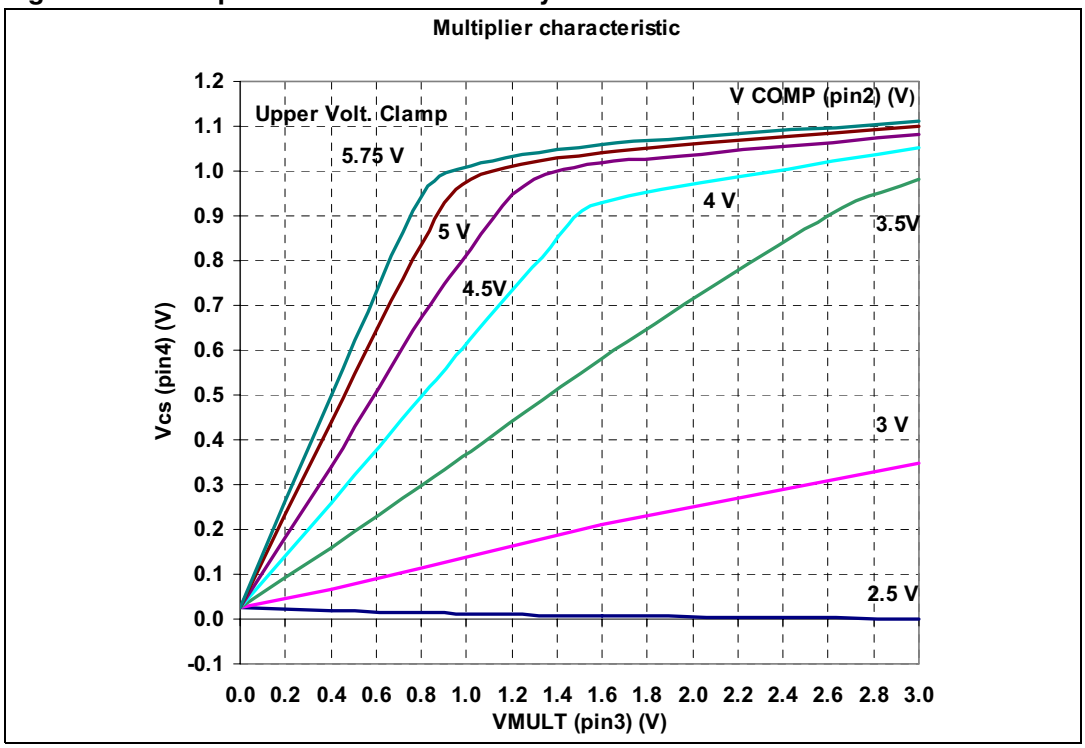
- Pin 3 (MULT): The MULT pin is the second multiplier input. It is connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference. The multiplier can be described by the relationship:

$$V_{CS} = k \cdot (V_{COMP} - 2.5\ V) \cdot V_{MULT} \tag{59}$$

where:

- V_{CS} (multiplier output) is the reference for the current sense
- k = 0.38 (typ) is the multiplier gain
- V_{COMP} is the voltage on pin 2 (E/A output)
- V_{MULT} is the voltage on pin 3

Figure 14. Multiplier characteristics family



A complete description is given in *Figure 14*, which shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed within the range 0 to 3 V of V_{MULT} and the range 0 to 1.16 V (typ) of V_{CS}, while the minimum guaranteed value of the maximum slope of the characteristics family (typ) is:

$$\frac{dV_{CS}}{dV_{MULT}} = 1.1\frac{V}{V} \tag{60}$$

Taking this into account, the following is the suggested procedure to properly set the operating point of the multiplier.

First, the maximum peak value for V_{MULT}, $VMULT_{max}$ is selected. This value, which occurs at maximum mains voltage, should be 3 V or nearly so in wide range mains and less in case of single mains. The sense resistor selected is R_s = 0.117 Ω and it is described in the paragraph concerning pin 4 of this section. The maximum peak value, occurring at maximum mains voltage, is:

$$VMULT_{max} = \frac{IL_{pksat} \cdot R_s}{1.1} \cdot \frac{VAC_{max}}{VAC_{min}}$$
$$VMULT_{max} = \frac{9.67A \cdot 0.117\ \Omega}{1.1} \cdot \frac{265Vac}{90Vac} = 3.02\ V \tag{61}$$

where IL_{pksat} and R_s have been already calculated, and 1.1 V/V is the multiplier maximum slope, as given in the datasheet.

From *(60)* the maximum required divider ratio is calculated as:

$$k_p = \frac{V_{MULT\,max}}{\sqrt{2}\cdot VAC_{max}} = \frac{3.02\ V}{\sqrt{2}\cdot 265 Vac} = 8.08\cdot 10^{-3} \quad (62)$$

Supposing a 300 µA current flowing into the multiplier divider the lower resistor value can be calculated:

$$R_{multL} = \frac{V_{MULT\,max}}{300\ \mu A} = \frac{3.02\ V}{300\ \mu A} = 10.03\ k\Omega \quad (63)$$

A commercial value of 10 kΩ for the lower resistor is selected. The upper resistor value can now be calculated:

$$R_{multH} = \frac{1-k_p}{k_p} R_{multL} = \frac{1-8.08\cdot 10^{-3}}{8.08\cdot 10^{-3}} 10\ k\Omega = 1.238\ M\Omega \quad (64)$$

In this application example R_{multH} = 1240 MΩ and a R_{multL} = 10 kΩ have been selected. Please note that for R_{multH} a resistor with a suitable voltage rating (> 400 V) is needed, or more resistors in series must be used.

The voltage on the multiplier pin with the selected component values re-calculated is 1.01 V at minimum line voltage and is 2.99 V at maximum line voltage. The multiplier works correctly within its linear region.

- Pin 5 (ZCD) is the input to the zero current detector circuit. It is connected to the line-modulated, fixed off-time circuit seen in the previous *Figure 6 on page 6*. Referring to *Section 3: The circuit implementing the line-modulated fixed off-time with the new L6562A*, the starting point for the design of the zero-current detector (ZCD) circuit is the pair of the desired values for T_{OFF} on the top of the line voltage sinusoid at minimum (T_{OFF} at VAC_{min}) and maximum line (T_{OFF} at VAC_{max}) obtained by setting the switching frequency on the peak of the sinusoid at low mains and considering the minimum on-time of the L6562A:

$$T_{OFF}(VAC_{min}) = \frac{k_{min}}{f_{sw\,min}} \qquad T_{OFF}(VAC_{min}) = \frac{0.32}{72\ kHz} - 220\ ns = 4.2\ \mu s \quad (65)$$

$$T_{OFF}(VAC_{max}) = \frac{T_{ONmin}\cdot k_{max}}{1-k_{max}} \qquad T_{OFF}(VAC_{max}) = \frac{450\ ns\cdot 0.94}{1-0.94} - 220\ ns = 6.8\ \mu s \quad (66)$$

where f_{swmin} is the switching frequency on the top of the sinusoid of the input voltage at VAC_{min} = 90 Vac (*Figure 15*).

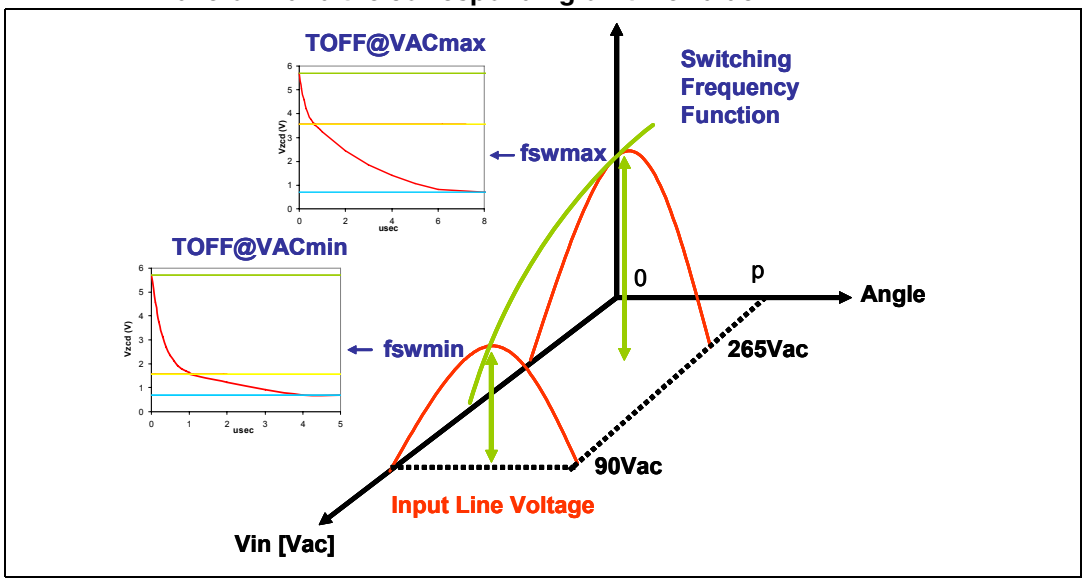
Let ρx as the ratio between *(66)*, *(65)*:

$$\rho_x = \frac{T_{OFF}(VAC_{max})}{T_{OFF}(VAC_{min})} \qquad \rho_x = \frac{6.8\ \mu s}{4.2\ \mu s} = 1.63 \tag{67}$$

In the formula *(65)*, *(66)* the delay between the ZCD signal and the gate drive signal is taken into account in order to increase the accuracy of the mathematical model.

From the theory of the line-modulation fixed off-time, T_{OFF} is increasing with the line voltage so that at maximum line voltage, the condition $T_{ON}>T_{ONmin}$ = 450 ns is always true for the L6562A [*4*]. This is important in order to avoid line distortion [*7*].

Figure 15. Switching frequency function on the peak of the sinusoid input voltage waveform and the corresponding off-time value



Now considering the two discharging resistors R and R_0 of the circuit of *Figure 6*, the ratio K_1 is defined:

$$K_1 = \frac{R}{R_0 + R} \tag{68}$$

where $0 < K_1 < 1$.Through the definition of the parameter K_2 it is underlined the expected time constant $\tau = (R//R_0)C$ necessary to achieve the desired T_{OFF} at 90 Vac.

$$K_2 = \frac{T_{OFF}(VAC_{min})}{\tau} \tag{69}$$

Finding a way to obtain K_1 and K_2 means increasing the values of R and R_0 and the discharging time constant of the capacitor C.

The following part describes the mathematical way to obtain the two parameters K_1 and K_2. Combining *(65)*, *(66)*, *(68)* and *(69)* with the expression of the off-time *(5)* the following expressions are obtained:

$$\rho(V_{multmin},k_1)=\frac{\left[\ln\left[\frac{\left[V_{multmin}\cdot\frac{VAC_{max}}{VAC_{min}}+V_F\right]\cdot(1-k_1)}{\left[V_{ZCDclamp}-\left[V_{multmin}\cdot\frac{VAC_{max}}{VAC_{min}}+V_F\right]\right]\cdot(k_1)}\right]^{1-k_1}+\ln\left(\frac{V_{ZCDtrigger}}{V_{multmin}\cdot\frac{VAC_{max}}{VAC_{min}}+V_F}\right)\right]}{\left[\ln\left[\frac{\left[V_{multmin}+V_F\right]\cdot(1-k_1)}{\left[V_{ZCDclamp}-\left[V_{multmin}+V_F\right]\right]\cdot(k_1)}\right]^{1-k_1}+\ln\left(\frac{V_{ZCDtrigger}}{V_{multmin}+V_F}\right)\right]} \quad (70)$$

$$k_2(V_{multmin},k_1)=\left[\frac{-1}{1-k_1}\cdot\ln\left[\frac{\left[V_{multmin}+V_F\right]\cdot(1-k_1)}{V_{ZCDclamp}-\left[V_{multmin}+V_F\right]\cdot k_1}\right]^{1-k_1}+\ln\left(\frac{V_{ZCDtrigger}}{V_{multmin}+V_F}\right)\right] \quad (71)$$

From *(70)* and *(71)*, solving the following equation:

$$\rho(V_{multmin},k_1)-\rho_x=0 \qquad K_1=0.91 \quad (72)$$

And then substituting the value of K_1 into the expression in *(70)*, the K_2 parameter is obtained:

$$K_2=k_2(V_{multmin},k_1) \qquad K_2=12.46 \quad (73)$$

From the values of K_1 and K_2 it is possible to calculate the time constant τ =(R1//R2) C necessary to achieve the desired T_{OFF} at 90Vac:

$$\tau=\frac{T_{OFF}(VAC_{min})}{K_2} \qquad \tau=\frac{4.2\ \mu s}{12.46}=336.7\ ns \quad (74)$$

Now selecting a capacitor C in the hundred pF or few nF, for example C =120 pF, it is possible to determine the required equivalent resistance value:

$$R_{eq}=\frac{\tau}{C} \qquad R_{eq}=\frac{336.7\ ns}{120\ pF}=2.81\ k\Omega \quad (75)$$

From *(67)* R and R_0 are found:

$$R=\frac{R_{eq}}{1-K_1} \qquad R=\frac{2.81\ k\Omega}{1-0.94}=31.5\ k\Omega \quad (76)$$

$$R_0 = \frac{R_{eq}}{K_1} \qquad R_0 = \frac{2.81\,k\Omega}{0.94} = 3.08\,k\Omega \tag{77}$$

Commercial values R = 30 kΩ and a R_0 = 3 kΩ have been chosen.

Figure 16 and *Figure 17* show the trend of the OFF-time and the switching frequency vs. the input mains voltage. The PFC inner current loop is working in the range 72 kHz - 132 kHz.

Due to the tolerance of the capacitor selected C and the two discharging resistors, it is important to take into account a variation on the switching frequency in a real board of about +- 10%.

Figure 16. Off-time vs. input mains voltage

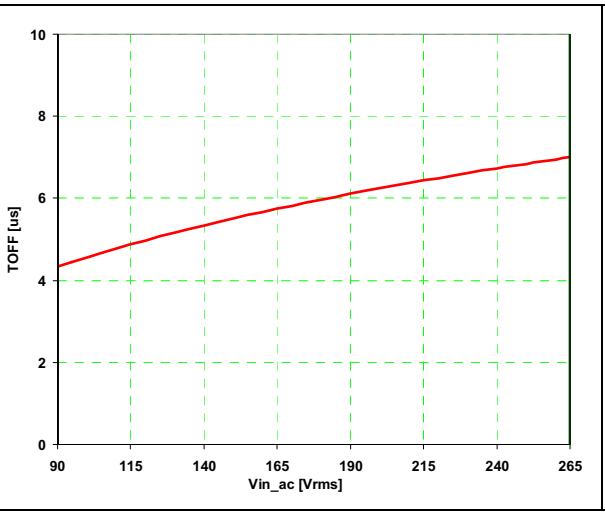
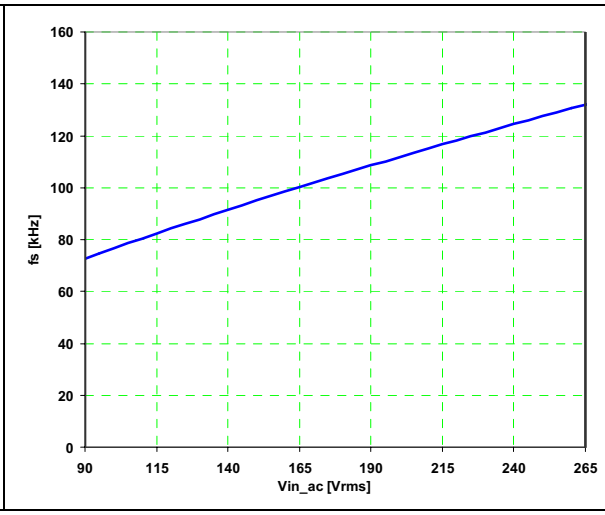


Figure 17. Switching frequency vs. input mains voltage



Finally the limiting resistor R_s should be selected according to the inequalities *(6)*.

$$\frac{15\,V - 5.7\,V - 0.6\,V}{10\,mA + \frac{5.7\,V}{2.81\,k\Omega}} < Rs < 2.81\,k\Omega \cdot \frac{10\,V - 5.7\,V - 0.6\,V}{5.7\,V} \tag{78}$$

and the speed-up capacitor C_s using *(7)*:

$$Cs < 120\,pF \cdot \frac{5.7\,V}{15\,V - 5.7\,V - 0.6\,V} \tag{79}$$

that means after algebra:

$$790\,\Omega < Rs < 1.94\,k\Omega \tag{80}$$

$$Cs < 78.6\ pF \quad (81)$$

A commercial value of the limiting resistor of 1.8 kΩ and a speed-up capacitor of 68 pF has been selected for this application.

- Pin 6 (GND): This pin acts as the current return both for the signal internal circuitry and for the gate drive current. When laying out the printed circuit board, these two paths should run separately.
- Pin 7 (GD) is the output of the driver. The pin is able to drive an external MOSFET with 600 mA source and 800 mA sink capability. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc. To avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the L6562A is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 1.1 V maximum on the pin (at Isink = 2 mA), with Vcc > VCC_ON. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET used for this purpose.
- Pin 8 (Vcc) is the supply of the device. This pin is externally connected to the startup circuit (usually, one resistor connected to the rectified mains) and to the self-supply circuit. Whatever the configuration of the self-supply system, a capacitor is connected between this pin and ground. To start the L6562A, the voltage must exceed the startup threshold (12.5 V typ). Below this value the device does not work and consumes less than 30 µA (typ) from Vcc. This allows the use of high value startup resistors (in the hundreds kΩ), which reduces power consumption and optimizes system efficiency at low load, especially in wide-range mains applications. When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 3.75 mA. The device keeps on working as long as the supply voltage is over the UVLO threshold (10.5 V max). If the Vcc voltage exceeds 25 V an internal Zener diode, 20 mA rated, is activated in order to clamp the voltage. Please remember that during normal operation the internal Zener does not have to clamp the voltage, in which case the power consumption of the device increases considerably and its junction temperature also increases. The suggested operating condition for safe operation of the device is below the minimum clamping voltage of the pin.

5 Design example using the L6562A FOT PFC Excel spreadsheet

An Excel spreadsheet has been developed to allow a quick and easy design of a boost PFC pre-regulator using the STM L6562A controller, operating in fixed off-time.

Figure 18 shows the first sheet already precompiled with the input design data used in the previous *Section 4: Designing a fixed off-time PFC*.

Figure 18. Excel spreadsheet design specification input table

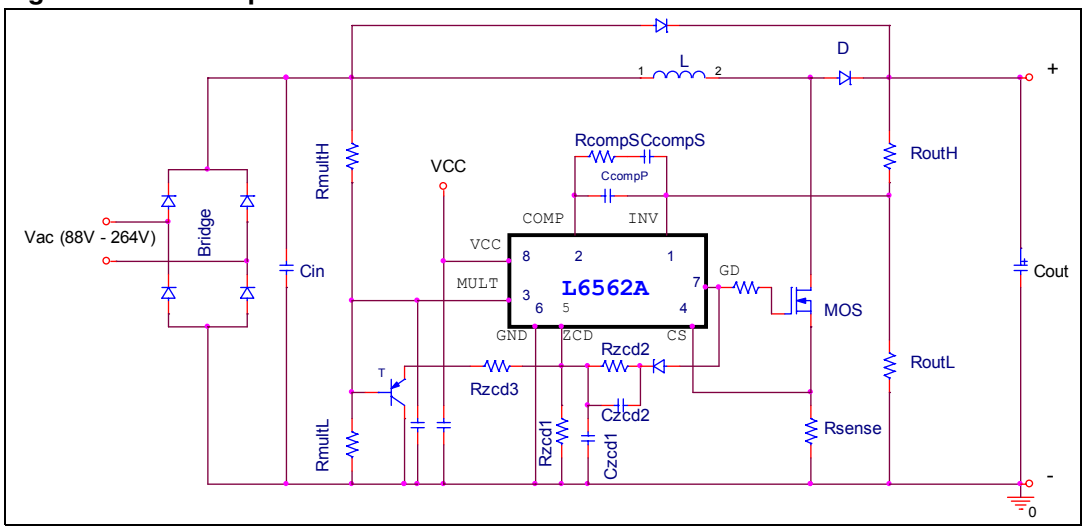
Parameter	Name	Value	Unit [ ]
Mains Voltage Range	VacMin	90	VACrms
Mains Voltage Range	VacMax	265	VACrms
Min.Mains Frequency	fl	47	Hz
Regulated Output Voltage	Vout	400	Vdc
Rated Output Power	Pout	400	W
Max. Output Low Frequency Ripple	Δ Vout	10	Vpk-pk
Max. Output Overvoltage	ΔOVP	40	Vdc
Holdup Capability	Thold	20	ms
Min. Output Voltage after Line drop	VoutMin	300	Vdc
Min. Switching Frequency:	fmin	72	kHz
Expected Efficiency	η	90	%
Expected Power Factor	PF	0.99	---
Max ind.curr.ripple to peak ratio VACmin,Pout_max)	Kr	0.34	---
Maximum Ambient Temperature	Tambx	50	C

Figure 19. Other design data

Parameter	Name	Value	Unit [ ]
Maximum Magnetic Flux Density	Bx	0.25	T
Ripple VoltageCoefficient	r	0.1	---

The tool is able to generate a complete part list of the PFC schematic represented in *Figure 20*, including the power dissipation calculation of the main components.

Figure 20. Excel spreadsheet FOT PFC schematic



The bill of material in *Figure 21* is automatically compiled by the Excel spreadsheet. It summarizes all selected components and some salient data.

Figure 21. Excel spreadsheet BOM

400	W FOT PFC BASED ON L6562A		
	BILL OF MATERIAL		
		Selected Value	Unit [ ]
BRIDGE RECTIFIER	D15XB60		
MOSFET P/N	2 x STP12NM50FP		
DIODE P/N	STTH8R06		
Inductor	Lx	500	µH
Max peak Inductor current	Ilpkx	9.67	A
Sense resistor	Rsx	0.12	Ω
Power dissipation	Ps	2.14	W
INPUT Capacitor	Cin	1	µF
OUTPUT Capacitor	Cout	330	µF
MULT Divider	Rmult L	10	kΩ
	Rmult H	1240	kΩ
ZCD set	Rzcd1	30	kΩ
	Rzcd2	1.8	kΩ
	Rzcd3	3	kΩ
	Czcd1	120	pF
	Czcd2	68	pF
Diode P/N	1N4148		
pnp-BJT P/N	BC857C		
Feedback Divider	RoutH	1530	kΩ
	RoutL	9.5	kΩ
Comp Network	CcompP	220	nF
	CcompS	2200	nF
	RcompS	47	kΩ
IC Controller	L6562A		

The following section is dedicated to report the main bench evaluation results of the 400 W FOT PFC with the L6562A available for the customer as an demonstration board.

6 EVL6562A-400W demonstration board

Figure 23 shows the schematic of an application board. It has been dimensioned using the Excel tool presented in *Section 5*.

The board implements a power factor correction (PFC) pre-regulator delivering 400 W, continuous power, on a regulated 400 V rail from a wide-range mains voltage and providing for the reduction of the mains harmonics, which complies with the European norm EN61000-3-2 or the Japanese norm JEIDA-MITI. This rail is the input for the cascaded isolated DC-DC converter that provides the output rails required by the load.

The board has been designed to allow full-load operation in still air.

Figure 22. EVL6562A-400W demonstration board

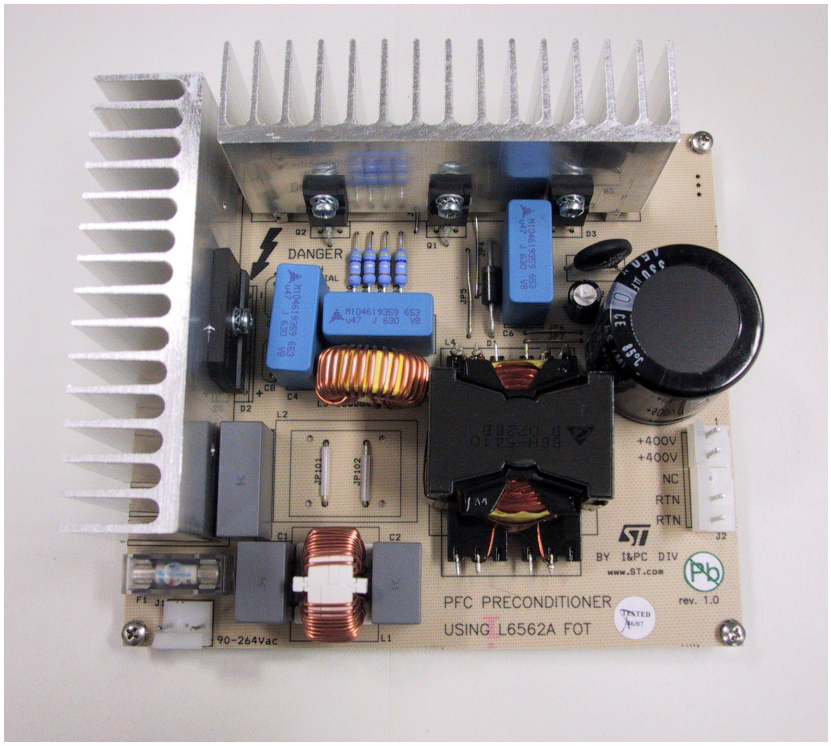
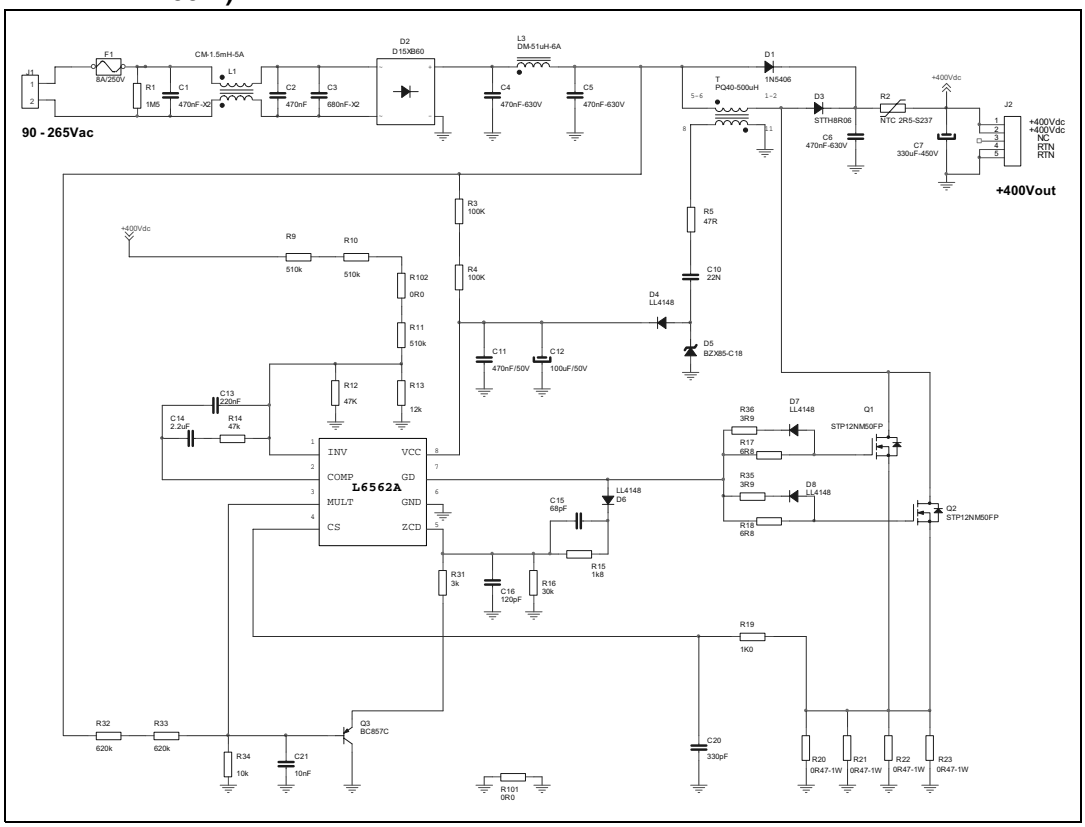


Figure 23. Wide-range 400 W demonstration board electrical circuit (EVL6562A-400W)



The power stage of the PFC is a conventional boost converter, connected to the output of the rectifier bridge D2. It includes the coil T, the diode D3 and the capacitors C6 and C7. The boost switch is represented by the power MOSFETs Q1 and Q2. The NTC R2 limits the inrush current at switch-on. It has been connected on the DC rail, in series to the output electrolytic capacitor, in order to improve the efficiency during low-line operation. Additionally, the splitting in two of output capacitors (C6 and C7) provides for managing the AC current mainly by the film capacitor C6 so that the electrolytic can be cheaper as it has just to bear the DC part.

At startup the L6562A is powered by the Vcc capacitor (C12) that is charged via the resistors R3 and R4, then the T secondary winding (pins 8-11) and the charge pump circuit (R5, C10, D5 and D4) generates the Vcc voltage powering the L6562A during the normal operations.

The divider R32, R33 and R34 provides the L6562A multiplier with the information of the instantaneous voltage that is used to modulate the boost current. The divider R9, R10, R11, R12 & 13 is dedicated to sense the output. The line-modulated FOT is obtained by the timing generator components D6, C15, R15, C16, R16, R31, Q3.

The board is equipped with an input EMI filter designed for a 2-wire input mains plug. It is composed of two stages, a common mode Pi-filter connected at the input (C1, L1, C2, C3) and a differential mode Pi-filter after the input bridge (C4, L3, C5). It also offers the possibility to easily connect a downstream converter.

7 Test results and significant waveforms

One of the main purposes of a PFC preconditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEIDA-MITI Class-D, at full load at both nominal input voltage mains.

As reported in the following *Figure 24*, *Figure 25*, *Figure 26* and *Figure 27* the circuit is able to reduce the harmonics well below the limits of both regulations from full load down to light load. Please note that all measures and waveforms have been done using a common mode Pi-filter connected at the input (C1, L1, C2, C3) and a differential mode Pi-filter after the input bridge for filtering the noise coming from the circuit.

Figure 24. EVL6562A-400W compliance to EN61000-3-2 standard at full load

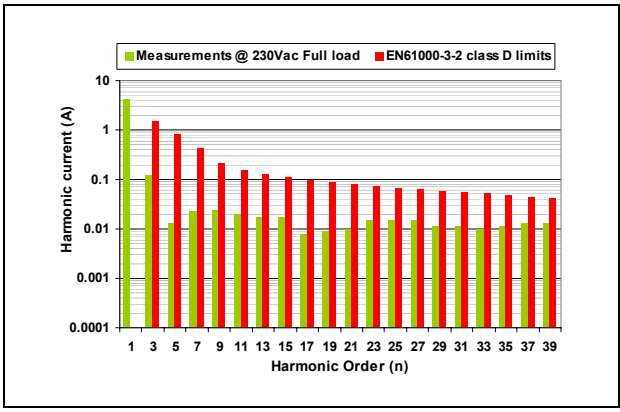


Figure 25. EVL6562A-400W compliance to JEIDA-MITI standard at full load

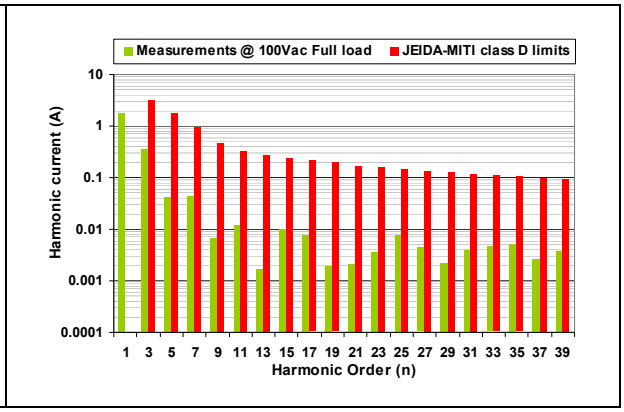


Figure 26. EVL6562A-400W compliance to EN61000-3-2 standard at 70 W

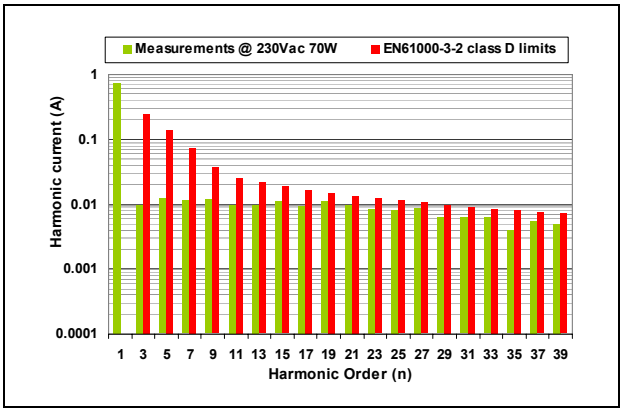


Figure 27. EVL6562A-400W compliance to JEIDA-MITI standard at 70 W

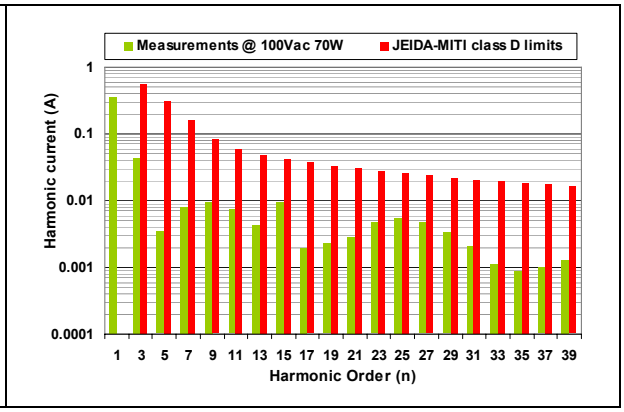


Figure 28. Power factor vs. Vin and load

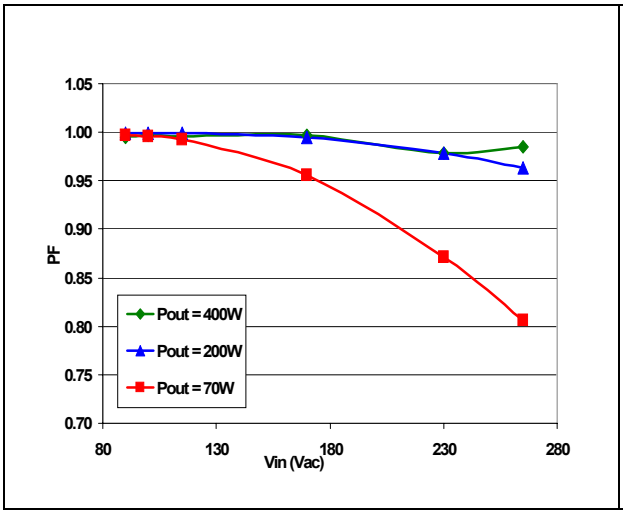


Figure 29. THD vs. Vin and load

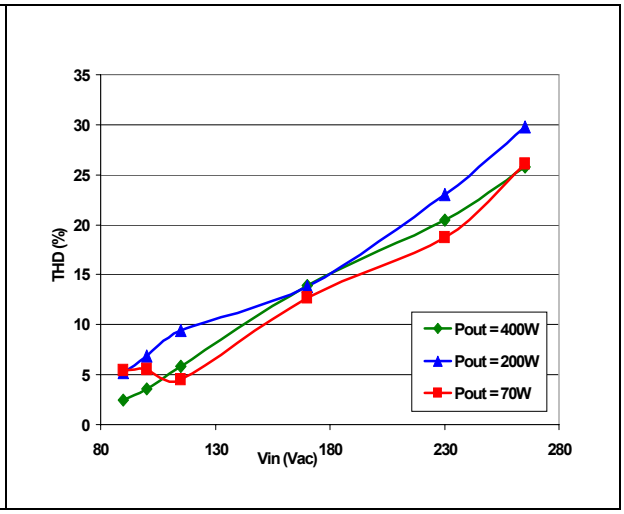


Figure 30. Efficiency vs. Vin and load

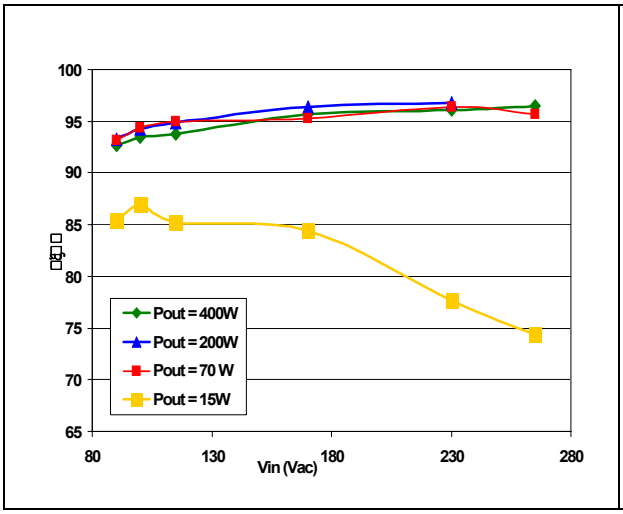
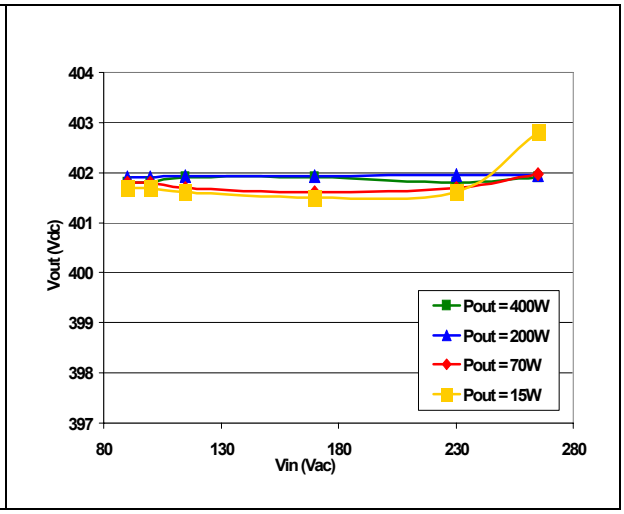


Figure 31. Static Vout regulation vs. Vin and load



The power factor (PF) and the total harmonic distortion (THD) have been measured too and the results are illustrated in *Figure 28*, *29*, *30*, *31*. As shown, the PF at full load and half load remains close to unity throughout the input voltage mains range while, when the circuit is delivering 70 W, it decreases at high mains range. THD is low, remaining within 30% at maximum input voltage.

The efficiency is very good at all load and line conditions. At full load it is always significantly higher than 90%, making this design suitable for high-efficiency power supplies.

The measured output voltage variation at different line and load conditions is shown in *Figure 28*, *29*, *30*, *31*. As shown, the voltage is perfectly stable over the entire input voltage range. Just at 265Vac and light load, there are negligible deviations of 1 V due to the intervention of the burst mode (for the “static OVP”) function.

For user reference, waveforms of the input current and voltage at the nominal input voltage mains and different load conditions are shown in *Figure 32* through *Figure 37*.

Figure 32. EVL6562A-400W: input current waveform at 100 V - 50 Hz - 400 W load

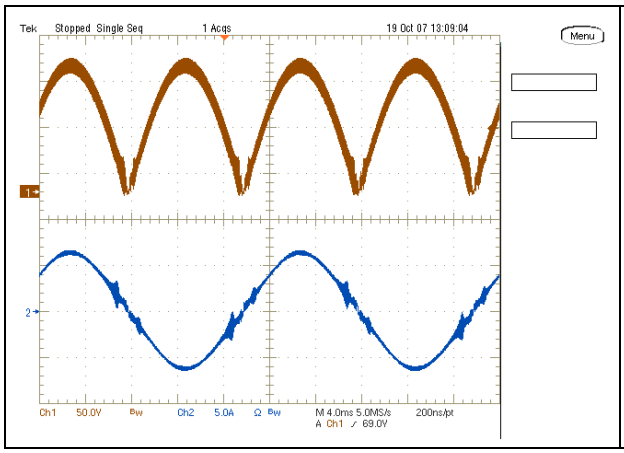


Figure 33. EVL6562A-400W: input current waveform at 230 V -50 Hz - 400 W load

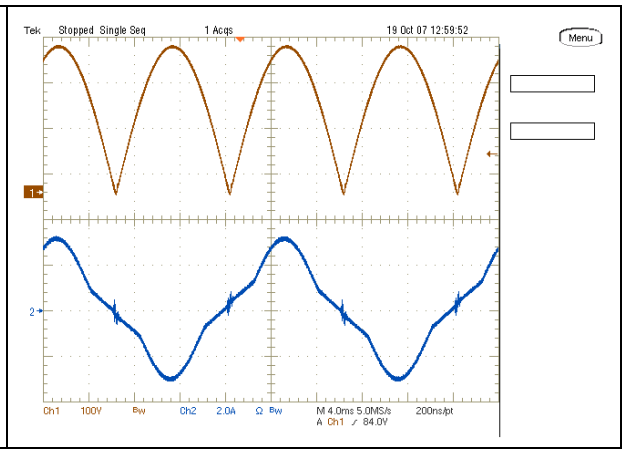


Figure 34. EVL6562A-400W: input current waveform at 100 V - 50 Hz - 200 W load

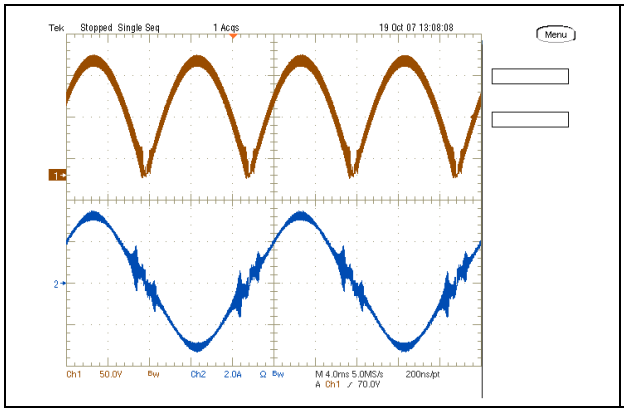


Figure 35. EVL6562A-400W: input current waveform at 230 V - 50 Hz - 200 W load

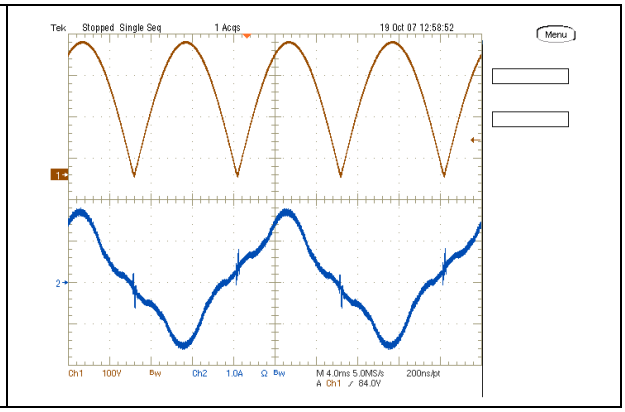


Figure 36. EVL6562A-400W: input current waveform at 100 V - 50 Hz - 70 W load

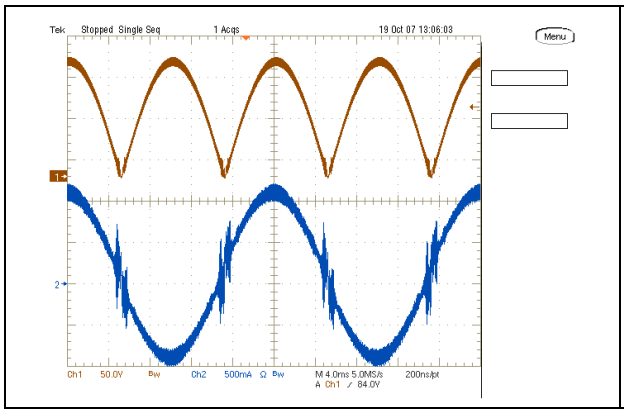
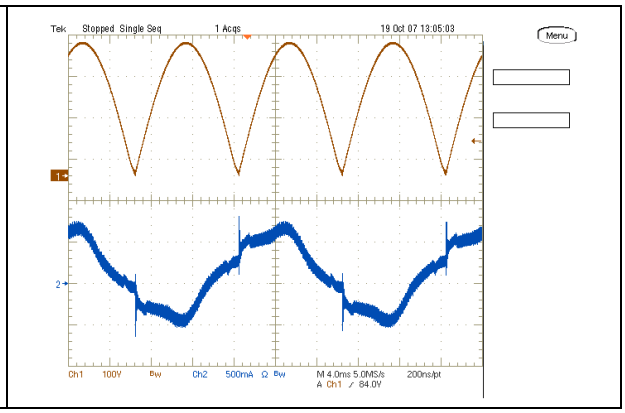


Figure 37. EVL6562A-400W: input current waveform at 230 V - 50 Hz - 70 W load



8 L6562A layout hints

The layout of any converter is a very important phase in the design process that sometimes does not get enough attention from the engineers. Even if it the layout phase sometimes looks time-consuming, a good layout does indeed save time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages which allows consistent cost savings.

The L6562A does not need any special attention to the layout, simply the general layout rules for any power converter must be carefully applied. Basic rules are listed below which can be used for other PFC circuits having any power level, working either in TM or with an FOT-control mode.

1. Keep power and signal RTN separated. Connect the return pins of components carrying high current such as input capacitors, sense resistors, or output capacitors as close as possible. This point is the RTN star point. A downstream converter or ballast must be connected to this return point.
2. Minimize the length of the traces relevant to the boost inductor, boost rectifier and output capacitor.
3. Keep signal components as close as possible to the L6562A pins. Specifically, keep the tracks relevant to pin #1 (INV) net as short as possible. Components and traces relevant to the error amplifier have to be placed far from traces and connections carrying signals with high dv/dt like the MOSFET drain.
4. Connect heat sinks to power GND.
5. Place an external copper shield around the boost inductor and connect it to power GND.
6. Please connect the RTN of signal components including the feedback and MULT dividers close to the L6562A pin #6 (GND).
7. Connect a ceramic capacitor (100÷470 nF) to pin #8 (Vcc) and to pin #6 (GND), close to the L6562A. Connect this point to the RTN star point 1.

9 Reference

1. “A New Continuous-Time Model for Current-Mode Control with Constant Frequency, Constant On-Time and Constant Off-Time, in CCM and DCM”, IEEE Power Electronics Specialists Conference Record, San Antonio, Texas, pp. 382-389, 1990
2. “Current Mode Control”, Venable Technical Paper #5, www.venableind.com
3. “Fixed off-time Control of PFC pre-regulators”, 10th European Conference on Power Electronics and Applications, EPE2003, Toulouse, France, paper 382
4. “L6562A, Transition-Mode PFC Controller”, datasheet, www.st.com
5. “Filter Inductor and Flyback Transformer Design for Switching Power Supplies”, UNITRODE Power Supply Design Seminar Manual, 1994 (SEM-1000)
6. “L6561, Enhanced Transition Mode Power Factor Corrector”, AN966, www.st.com
7. “Design fixed off-time controlled PFC pre-regulators with the L6562”, AN1792
8. “400W FOT-controlled PFC pre-regulator with the L6563”, AN2485
9. “A systematic Approach to Frequency Compensation of the Voltage loop in boost PFC pre-regulator”, Abstract
10. “Control loop modelling of L6561-based TM PFC”, AN1089

10 Revision history

Table 1. Document revision history

Date	Revision	Changes
20-Aug-2008	1	Initial release
05-Mar-2010	2	Updated Coverpage, *Section 3* and equation *(28)*

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